Abstract of the Disclosure

An MOS device includes a semiconductor layer of a first conductivity type, a source region of a second conductivity type formed in the semiconductor layer, and a drain region of the second conductivity type formed in the semiconductor layer and spaced apart from the source region. A gate is formed proximate an upper surface of the semiconductor layer and at least partially between the source and drain regions. The MOS device further includes a buried LDD region of the second conductivity type formed in the semiconductor layer between the gate and the drain region, the buried LDD region being spaced laterally from the drain region, and a second LDD region of the first conductivity type formed in the buried LDD region and proximate the upper surface of the semiconductor layer. The second LDD region is self-aligned with the gate and spaced laterally from the gate such that the gate is non-overlapping relative to the second LDD region.